Advanced Multiphysics Integration Technologies and Designs

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Oak Ridge National Laboratory

2018 U.S. DOE Vehicle Technologies Office Annual Merit Review

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Overview

Timeline

- Start – FY18
- End – FY20
- 17% complete

Barriers

- Availability and the limited field reliability data of wide band-gap (WBG) power devices
- Meeting DOE ELT 2025 High Voltage Power Electronics Targets
  - Power Density: 100 kW/L
  - Cost: $2.7/kW
  - Peak Efficiency: > 97%
  - Reliability: 300,000 mile lifetime or 15 years

Budget

- Total project funding
  - DOE share – 100%
- Funding received in FY17: N/A
- Funding for FY18: $700K

Partners

- Momentive, Henkel, and Indiana IC
- NREL
- ORNL – Emre Gurpinar, Jordan Besnoff, Steven Campbell, Tong Wu, and Burak Ozpineci

Any proposed future work is subject to change based on funding levels

Project Objective and Relevance

- Overall Objective
  - Develop technologies for next generation advanced integrated power electronic systems enabling high power density and reliability to achieve DOE ELT 2025 technical targets (100 kW/L, $2.7/kW, and 300,000 mile lifetime)
- FY18 Objectives
  - Power Module Design:
    - Evaluate thermal performance and design challenges of insulated metal substrate (IMS) with Thermal Pyrolytic Graphite (TPG) insert as a substrate solution
    - Evaluate feasibility of Quilt Packaging (QP) as an interconnect solution in power modules
  - Gate Driver and Auxiliary Components:
    - Develop radio frequency (RF) based solutions for ultra compact isolated signal and power transfer
    - Develop low profile, high power density, and isolated compact DC/DC converter designs for conventional gate drive supply

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Milestones

Date	Milestones and Go/No-Go Decisions	Status
Dec. 2017	Milestone: Identify state-of-the-art isolated DC/DC converter and RF coupler topologies	Completed
March 2018	Milestone: Finalize theoretical analysis and fundamentals of DC/DC converter and RF coupler	Completed
June 2018	Go/No-Go Decision: If the simulation and theoretical analysis results indicate the functionality, compactness, and potential to meet DOE ELT 2025 targets, then start optimization and advanced modelling	On Track
Sept. 2018	Milestone: Finalize the simulation and theoretical based optimization	On Track

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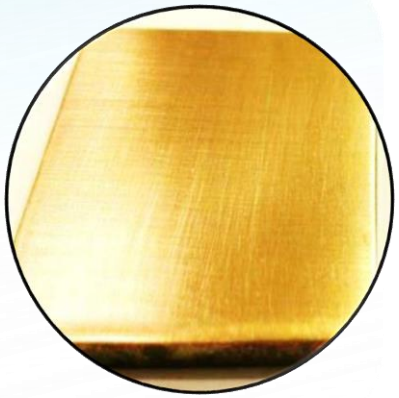
Approach/Strategy

- Increase power density and reliability of power electronics to meet DOE ELT 2025 targets (100 kW/L, and 300,000 mile lifetime) by focusing on power electronic module research

Power Electronic Module Research

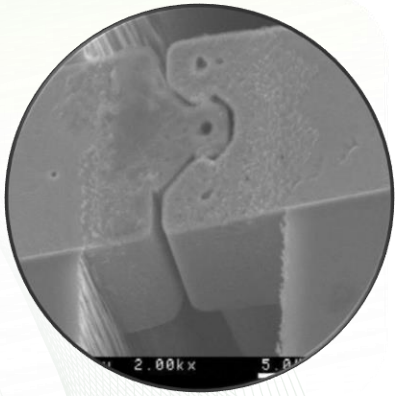
Substrates for Power Electronic Modules

- Identify state-of-the-art (SOA) substrate solutions that allow increased power density and high reliability for WBG device based power modules via
  - Better coefficient of thermal expansion (CTE) matching between WBG devices and power module materials
  - Improved heat extraction
  - Enhanced thermal and power cycling capability



Interconnects with High Power Density

- Evaluate and introduce low profile, high current density reliable chip-to-chip, and chip-to-package interconnects for power modules and auxiliary circuits (e.g. gate drivers) which will enable
  - Reduced parasitic inductance in the system for optimum switching performance
  - Reduced power module size
  - Enhanced reliability by moving to wire bondless solutions



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Images are courtesy of Momentive and Indiana IC

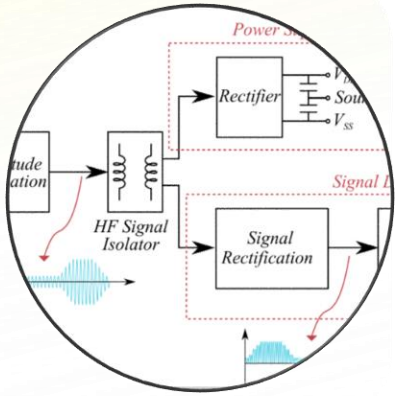
Approach/Strategy

- Increase power density and reliability of power electronics to meet DOE ELT 2025 targets (100 kW/L, and 300,000 mile lifetime) by focusing on gate driver research

Gate Driver Research for WBG Devices

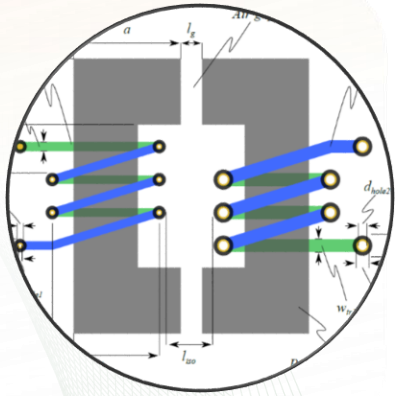
Compact Signal and Power Transfer for Gate Drivers

- Develop novel architectures for combined signal and power transfer with advanced functionalities for gate drivers to achieve
  - High power density by minimizing auxiliary components
  - Integration of gate drive circuitry to WBG modules
  - Advanced gate drive functionality for improved EMI, short circuit protection and loss distribution



Compact Power Isolation and Transfer for Auxiliaries

- Design and optimize low profile, isolated, high power density DC/DC converters to enhance overall power density of gate drivers for WBG devices by
  - High frequency operation to minimize passive components (e.g. isolation transformer)
  - Soft switching for active switches to maintain high efficiency
  - Optimized and controlled parasitic (e.g. coupling capacitance) design



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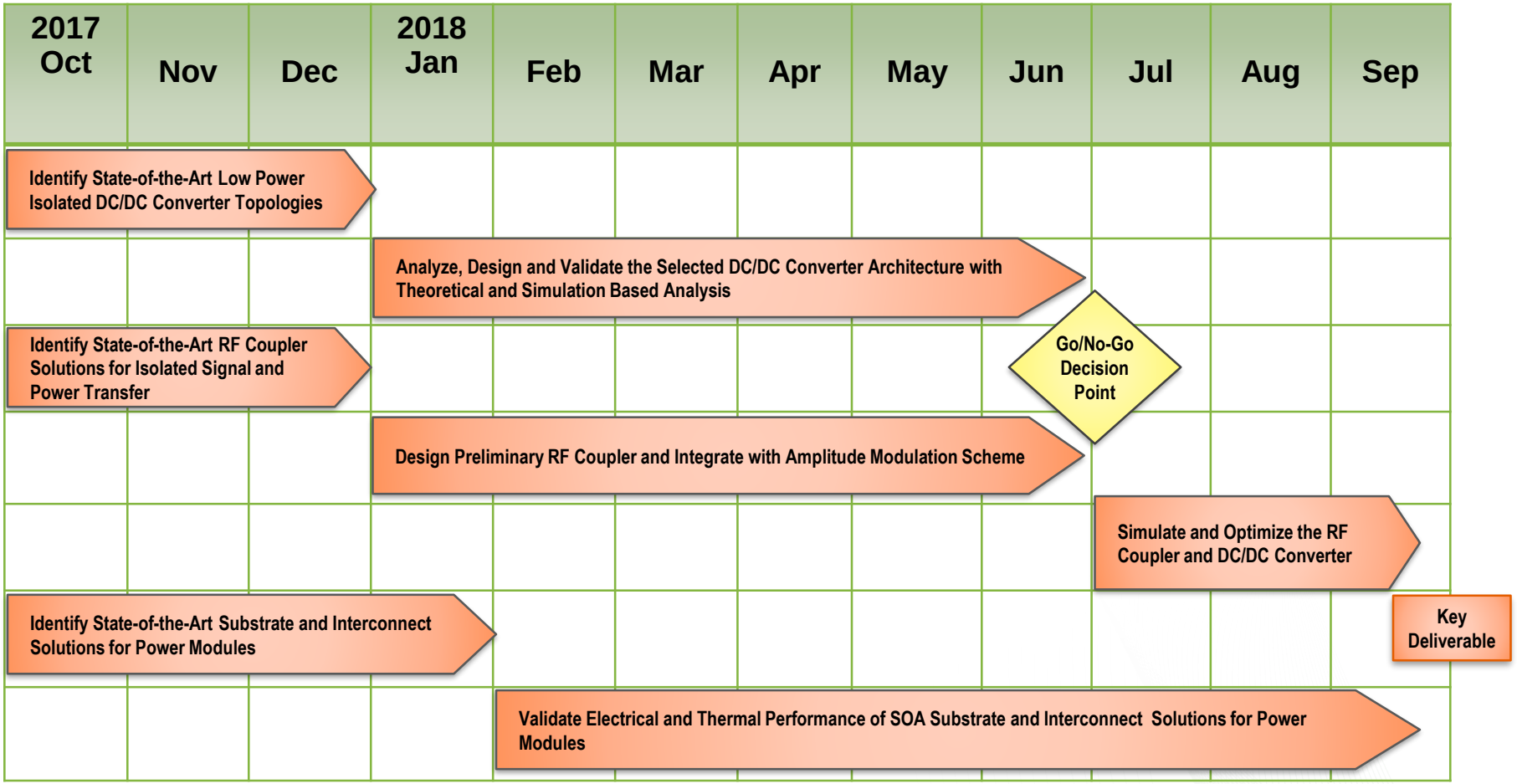
Approach FY18 Timeline



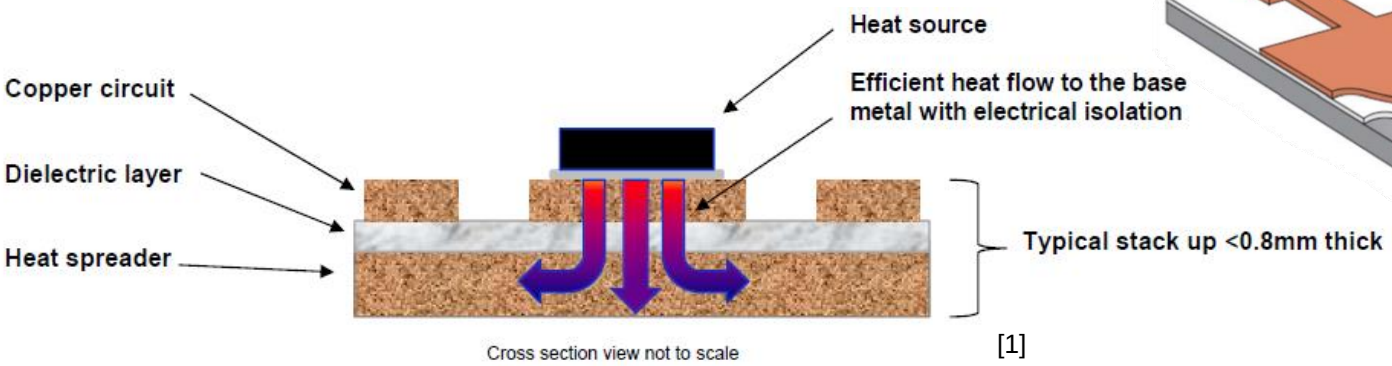
Go/No-Go Decision Point: If the simulation and theoretical analysis results indicate the functionality, compactness, and potential to meet DOE ELT 2025 targets, then start optimization and advanced modelling

Key Deliverable: Performance parameters and metrics of compact isolated signal and power transfer solutions

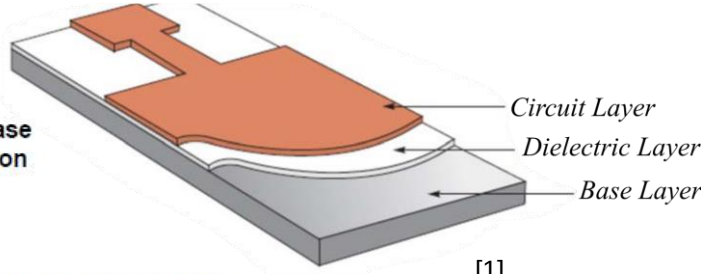
Any proposed future work is subject to change based on funding levels

Technical Accomplishments – FY18

Identified SOA Insulated Metal Substrate (IMS)



[1]

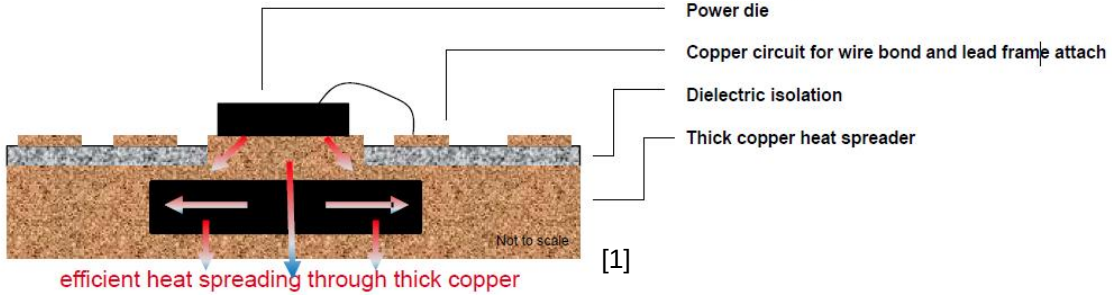


[1]

- Formed by metal baseplate, insulating sheet and thick copper foil on top. Traditional IMS structure has low fabrication cost and high thermal resistance in comparison to DBC
- The CTE of the composite is determined by metal encapsulant and independent of TPG loading

Material	In-Plane TC (W/m-K)	In-Plane CTE (ppm/°C)	Specific Gravity
Aluminum	210	24	2.7
Copper	400	16	8.9
AlSiC	180	9.5	3.0
WCu	190	8.3	15.6
MoCu	170	9.0	9.8
TPG	1500+	-1	2.3

[2]



[1]

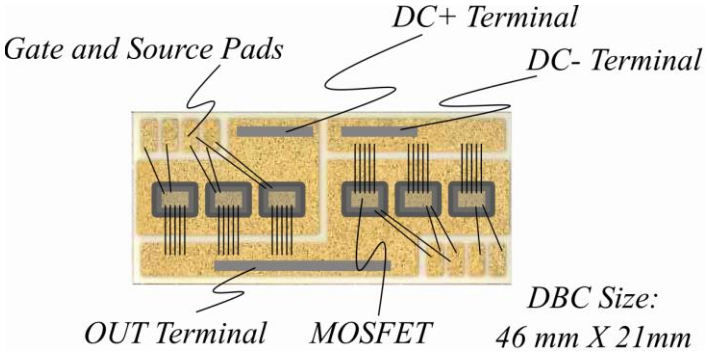
- IMS with TPG insert is a promising substrate for WBG power modules

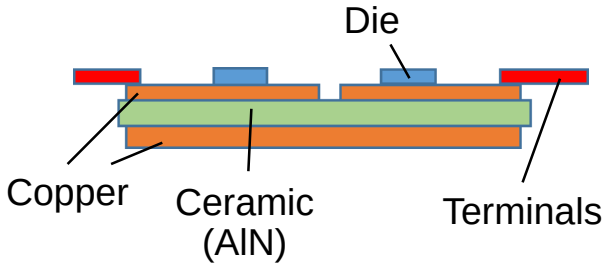
[1] Henkel
[2] Momentive

Technical Accomplishments – FY18

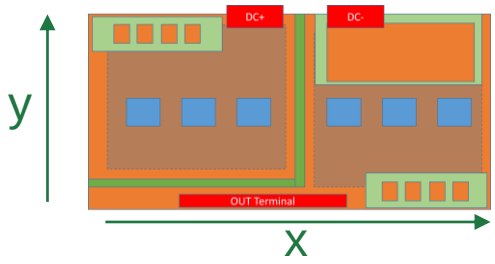
Designed IMS with TPG Insert

ORNL DBC Based Solution

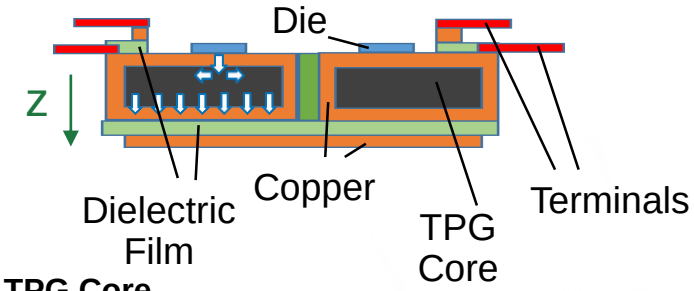




IMS with TPG Insert Based Solution



* Drawings not to scale



Thermal Conductivity of TPG Core

Y-Z	Total Thickness	TPG Thickness	TC-in plane (x)	TC-in plane (y)	TC-thru plane (z)
	mm	mm	W/m-K	W/m-K	W/m-K
Copper	1.60		396	396	396
TMP-EX	1.60	1.10	131	1155	802

[1]

[1] Momentive

- Same electrical layout is used for the comparison
- Future improvement on CTE matching to WBG devices can be accomplished by using low CTE metal to encapsulate TPG insert
- Thermal performance of DBC and IMS with TPG insert will be compared

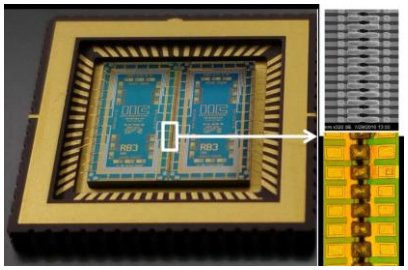
Technical Accomplishments – FY18

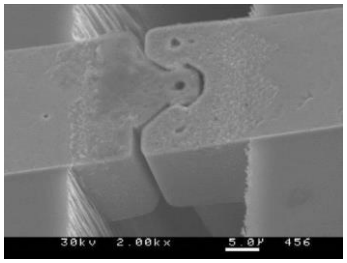
Identified Low Inductance, High Density SOA Interconnects

- Quilt Packaging: chip-to-chip interconnect technology that incorporates conductive metal “nodules” on the sides of the chips

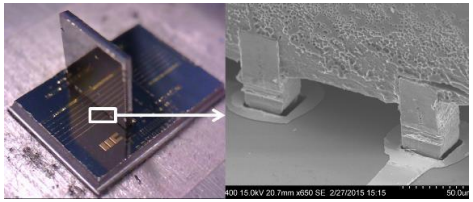
Quilt Packaging Examples in Microelectronics

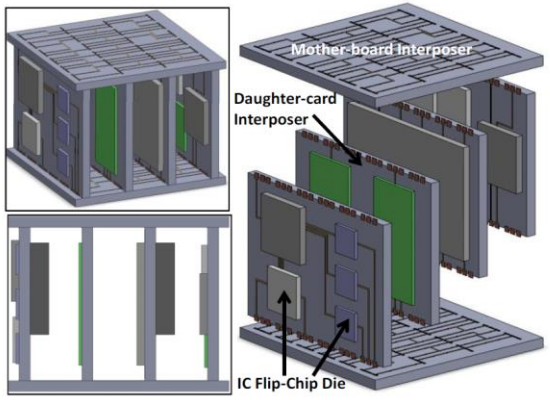
Chip-to-chip Interconnects





Board-to-board Interconnects





- Solid metal, typically Cu
  - Width: 5 to 500 μm
  - Thickness: 20-50 μm
  - 10 μm nodule pitch possible
- Increased power density
- Robust electrical and mechanical interconnects
- Reduced interconnect parasitic
- High density 3D integration of gate drivers and auxiliary circuits

Source: Indiana IC

Indiana Integrated Circuits LLC

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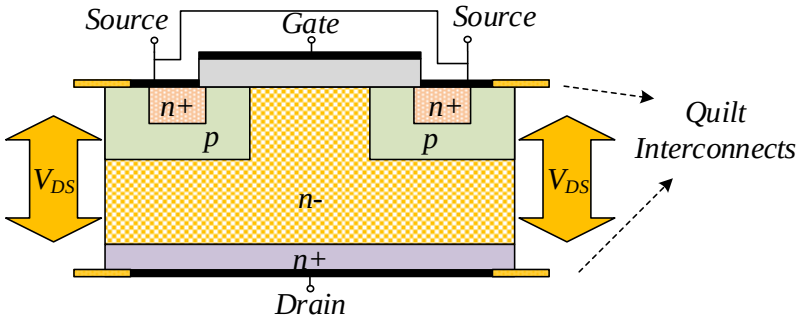
Technical Accomplishments – FY18

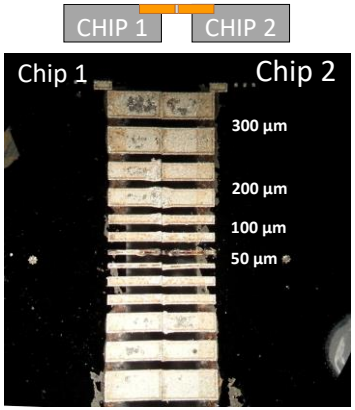
Applying Quilt Packaging to Power Electronics

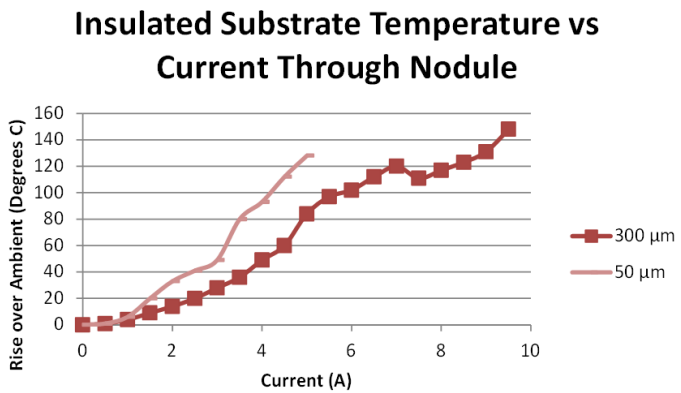
- Chip to chip interconnect challenges
  - High voltage stress across interconnects in vertical devices (e.g. SiC DMOSFET) has to be addressed



    - QP samples will be simulated and analyzed for high voltage withstand capability.
  - Several quilt based interconnects on Si substrate without active power devices have been analyzed by Indiana IC for high current conduction capability

Device Under Test





Source: Indiana IC

Indiana Integrated Circuits, LLC

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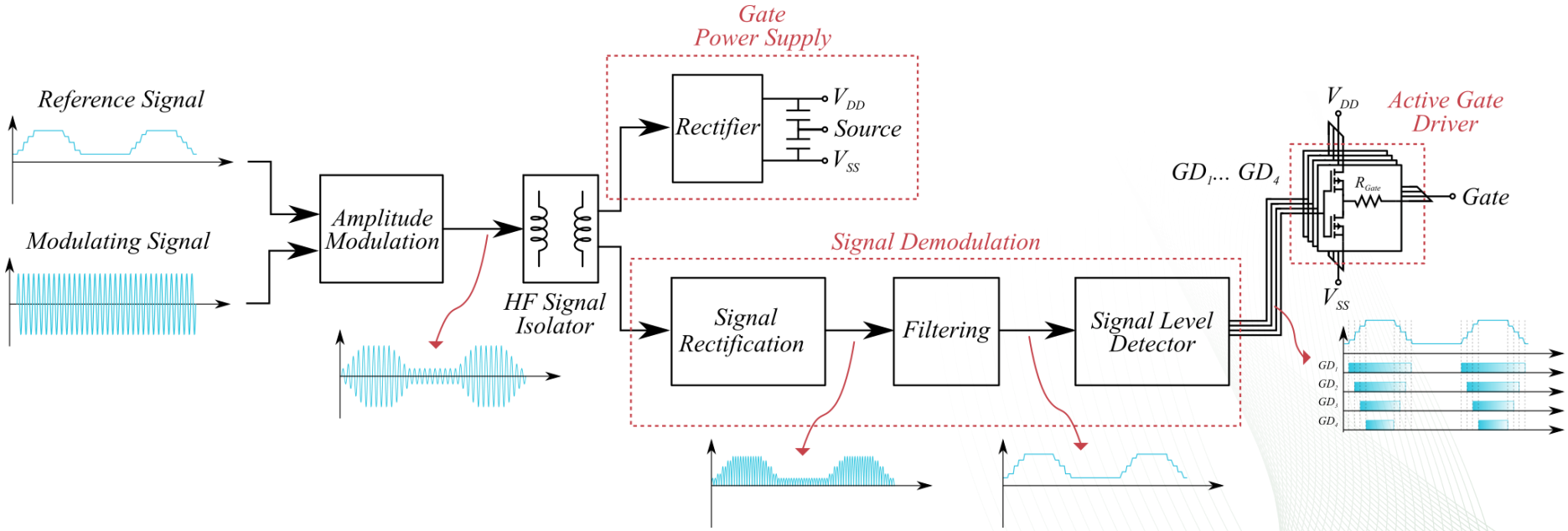
Technical Accomplishments – FY18

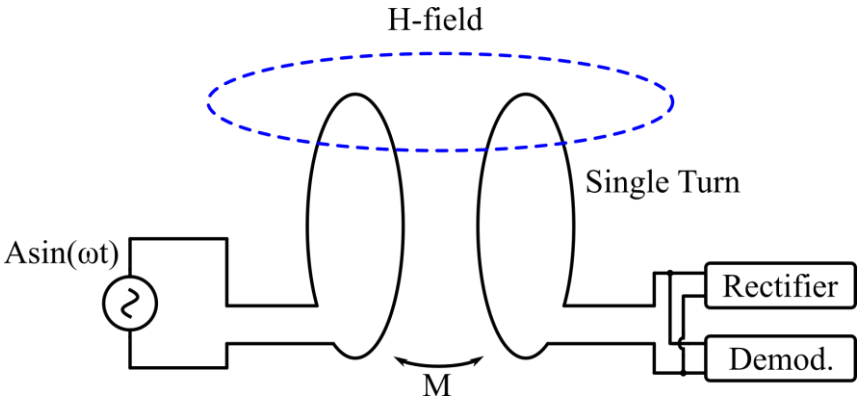
Proposed Compact Signal and Power Transfer for Gate Drivers

- Conventional gate drivers use separate signal and power isolators with limited power density and dV/dt immunity
- Novel RF based isolator is proposed which combines isolated gate signal, gate impedance and power transfer
  - The fixed frequency of the signal provides easier RF coupler design
  - Amplitude of the signal provides gate signal and impedance information



Technical Accomplishments – FY18
Analyzed RF Based Inductive Coupler

- Utilize near-field inductive coupling via coupled coils
  - Easily printable & low-profile (standard printed circuit board techniques)
  - Design can be easily tailored for efficiency, frequency, capacitance, and isolation
  - Operate on near-field inductive coupling
    - Naturally strong EMI immunity: close coupling & coil filtering effects
    - Unaffected by most PCB substrates (typically $\mu_r \approx 1$)
  - Have been shown to support both power & high bandwidth communication with high efficiency ([2] & [3])

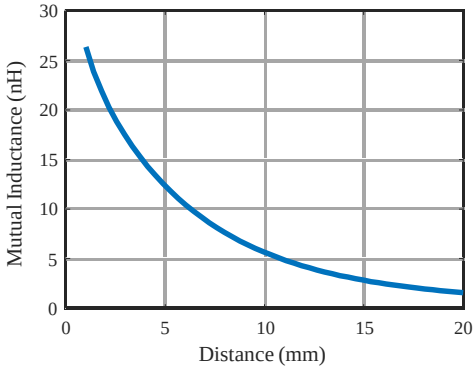


Coil inductance

$$M = k\sqrt{L_1 L_2}$$

Coupling coefficient

Mutual Inductance for 2 coils of 10 mm radius



[2] J. Besnoff and D. Ricketts. "Wide Bandwidth for High-Speed Communication in Mid-range, Resonant WPT and RFID Systems" in 2015 European Microwave Conference (EuMC), p. 147-150, 2015.
[3] Besnoff *et al*. "Ultrahigh-Date-Rate Communication and Efficient Wireless Power Transfer at 13.56 MHz" in IEEE Antennas and Wireless Propagation Letters, Vol. 16, pp. 2634-2637, 2017.

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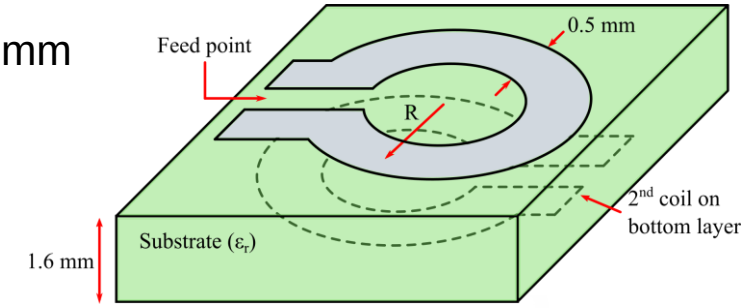
Technical Accomplishments – FY18

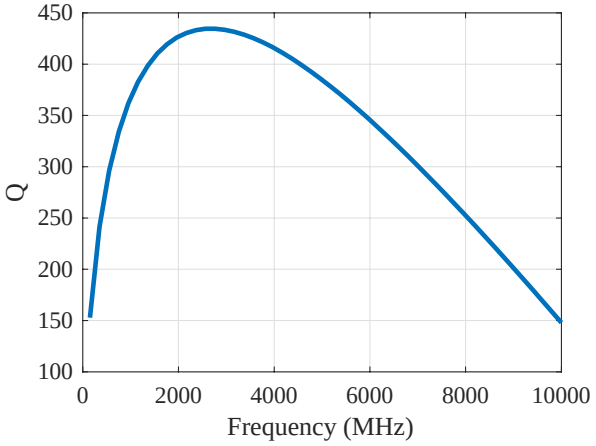
Analyzed RF Based Inductive Coupler

- Loop circumference equal to 1/10th of signal wavelength (λ/10) ensures uniform current and strong magnetic coupling
- Quality(Q)-factor trend due to increasing loop resistance and decreasing inductance as loop scales with frequency
- At standard PCB substrate (FR4) thickness of 1.6 mm
  - Achieved > 90% up to 4 GHz in theoretical analysis
  - At 4 GHz
    - Coil radius (R) = 0.57 mm
    - Estimated parasitic capacitance C_p = 0.044 pF

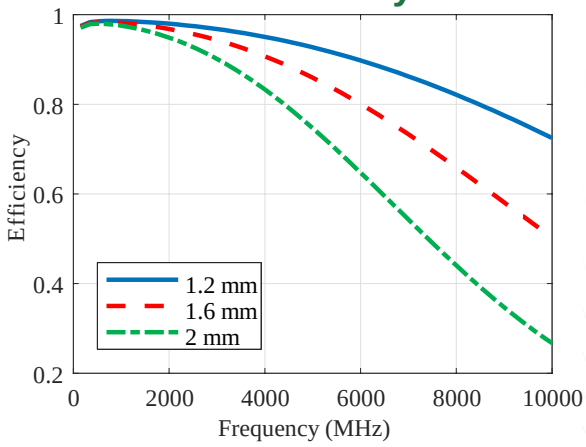
Inductive Coupler



Quality Factor



Efficiency



$$\text{Coil Radius} = \frac{3 \times 10^8}{20\pi f \sqrt{\varepsilon_r}} \text{ [m]}$$

f: Signal frequency
ε_r: Relative permittivity

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Technical Accomplishments – FY18

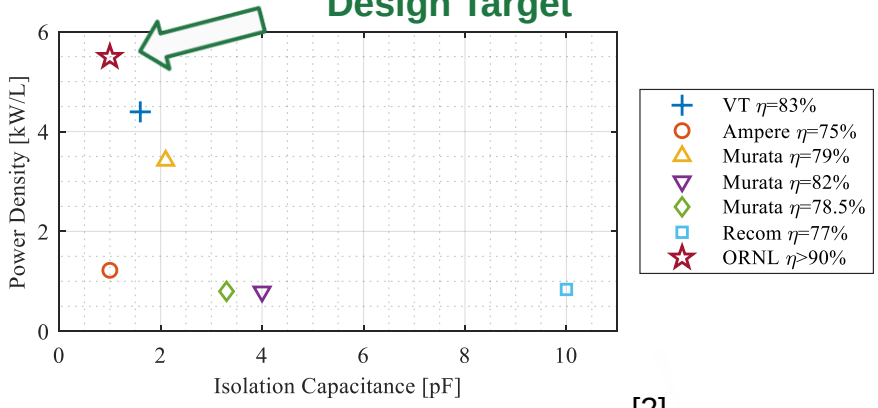
Proposed Compact Isolated DC/DC Converter

- Commercial gate drivers have high coupling capacitances with low power densities.
- A 3 W isolated DC/DC converter with high power density (> 5.5 kW/L) and low coupling capacitance (< 1 pF) was chosen as the optimization design target.

Proposed Isolated DC/DC Converter Design Targets

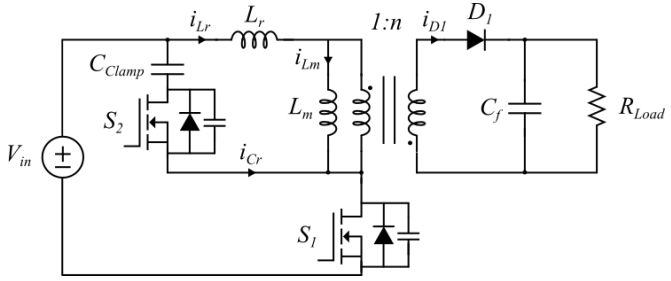
Definition	Symbol	Value
Output Voltage	V_{out}	20 V
Input Voltage	V_{in}	5 V
Output Power	P_{out}	3 W
Efficiency Target	η	> 90 %
Coupling Capacitance	C_p	< 1 pF
Power Density Target	p_{conv}	5.5 $\frac{\text{kW}}{\text{lt}}$ (90 $\frac{\text{W}}{\text{in}^3}$)
Switching Frequency	f_{sw}	500 kHz - 10 MHz

SOA Power Supplies and Design Target



[2]

Chosen Architecture for Optimization: Active Clamp Flyback



Active clamp flyback converter [1] is chosen as the suitable topology to be optimized according to design targets

- Two active switches at the primary side with zero-voltage-switching (ZVS) (suitable for GaN HEMTs)
- No active switch on the secondary side and zero-current-switching (ZCS) operation of the output diode
- Discontinuous current mode operation (smaller transformer size)
- Fixed frequency operation

[1] R. Perrin, N. Quentin, B. Allard, C. Martin and M. Ali, "High-Temperature GaN Active-Clamp Flyback Converter With Resonant Operation Mode," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 3, pp. 1077-1085, Sept. 2016.
[2] B. Sun, R. Burgos and D. Boroyevich, "2 W Gate drive power supply design with PCB-embedded transformer substrate," *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, 2017, pp. 197-204.

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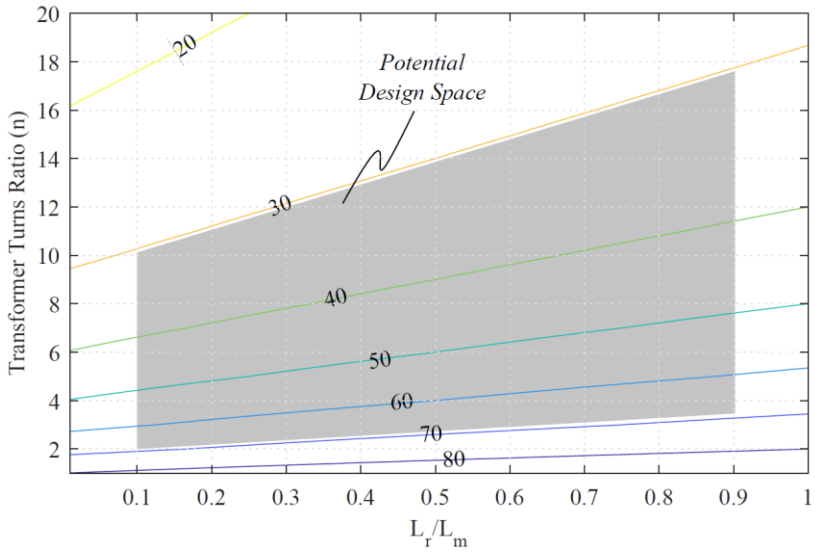
Technical Accomplishments – FY18

Developed Design Methodology for Converter Analysis

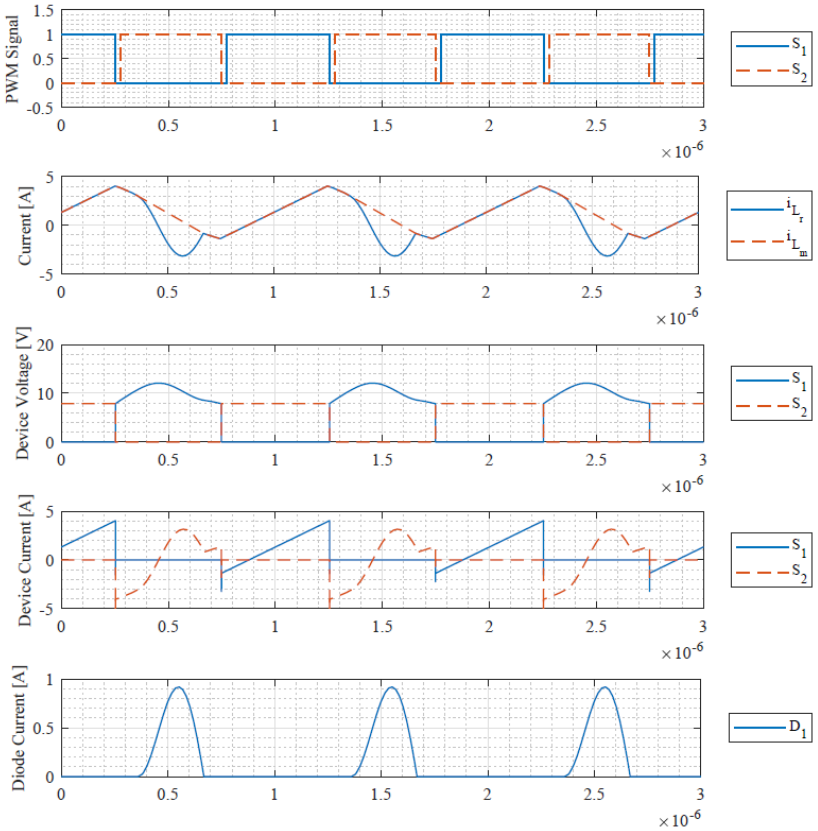
- The developed methodology is used to select suitable passive components (C_{Clamp}, L_r, L_m) in a given design space

Duty Cycle for L_m/L_r vs turns ratio at V_{OUT}/V_{IN}=4



- Potential design space is determined based on converter gain, turns ratio, duty cycle, and transformer coupling factor

Verified Functionality and Approach at f_{sw}= 1 MHz



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Technical Accomplishments – FY18

Proposed Approach for Transformer Analysis and Design

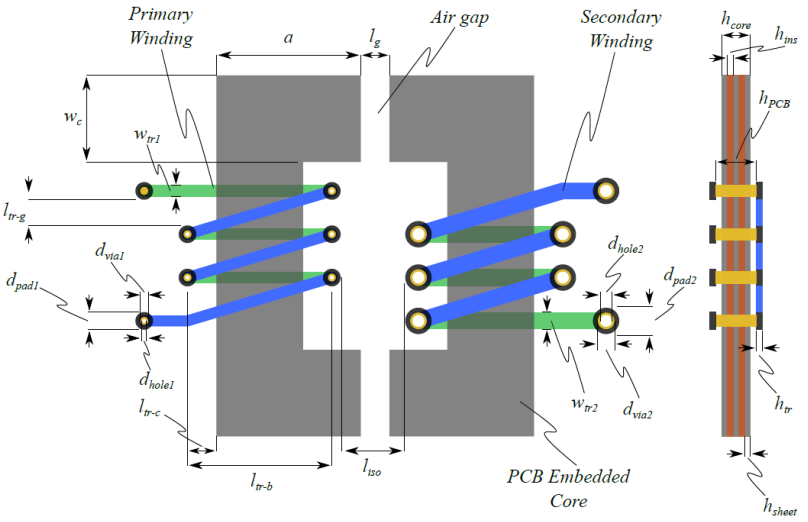
- Gate driver isolation transformer structure in the proposed topology has been modelled for size optimization with respect to given operating conditions (power, turns ratio, core permeability etc.)

Transformer Design Parameters (Lm, Lr, n, C_p etc.)

Winding Parameters:

- Primary and secondary current waveforms
- Winding resistance at given frequency
- PCB manufacturing constraints (e.g. track width, clearance)

Transformer model including winding and core losses, and physical dimensions



Core Parameters:

- B-H curve
- Power Loss
- Mechanical and manufacturing constraints (e.g. minimum core area, thickness)

Transformer volume; winding and core losses

Responses to Previous Year Reviewers' Comments

- This project is a new start

Reviewer comment: N/A

Response/Action: N/A

Collaboration and Coordination with Other Institutions

Organization	Role
MOMENTIVE, BERGQUIST, Henkel	IMS with TPG Insert Design and Manufacturing
Indiana Integrated Circuits, LLC	Quilt Packaging Interconnect Design and Evaluation
NREL NATIONAL RENEWABLE ENERGY LABORATORY	Thermal Analysis

Remaining Challenges and Barriers for FY18

- Insulation of Quilt Packaging for high voltage operation
  - Different encapsulation materials will be applied
  - Dielectric breakdown characterization will be conducted
- Impact of parasitic components to the operation of RF coupler
  - Finite element analysis simulation of RF coupler in Ansys HFSS will be conducted
- Achieving high efficiency in RF coupler with harmonic content coming from gate driver power supply
- Obtaining ferrite transformer core loss data with non-sinusoidal excitation for MHz range operation, and bespoke core shape for PCB embedding

Any proposed future work is subject to change based on funding levels

Proposed Future Work

- **Remainder of FY18**
  - Prototype IMS with TPG insert and compare with DBC under different loading conditions
  - Evaluate various encapsulants for Quilt Packaging and voltage withstand capability of Quilt Packaging
  - Simulate RF coupler in Ansys HFSS to verify convergence/ proper meshing
  - Integrate RF coupler with amplitude modulation scheme
  - Introduce core loss and coupling capacitance equations into DC/DC converter for transformer modelling and optimization
  - Introduce semiconductor loss into DC/DC converter model for pareto-front optimization of the system
- **FY19**
  - Optimize and prototype isolated DC/DC converter
  - Prototype amplitude modulation and demodulation for RF coupler
  - Design and simulate active gate drive with RF coupler
  - Optimize of IMS with TPG insert for 100 kW traction inverter
  - Embed Quilt Packaging into high voltage vertical devices

Any proposed future work is subject to change based on funding levels

Summary

- **Relevance:** DOE ELT 2025 high voltage power electronics targets require revisiting the conventional Silicon oriented integration to enable the benefits of WBG devices, and to achieve power density, cost and reliability targets
- **Approach:** Develop substrate, interconnect technologies for power modules, and signal and power isolation technologies for gate drivers to achieve high power density and reliability in next generation advanced integrated power electronic systems
- **Collaborations:** Momentive, Henkel, Indiana IC, NREL
- **Technical Accomplishments:**
  - Evaluated and designed IMS with TPG insert for WBG power modules
  - Evaluated and reviewed of Quilt Packaging as a wire bond alternative for power electronic interconnects
  - Proposed and preliminary designed a novel RF based isolated signal and power transfer
  - Conducted theoretical and simulation based analysis of a isolated low power, high frequency DC/DC converter for gate driver systems
- **Future Work:**
  - Prototype, characterize and optimize IMS with TPG core
  - Characterize high voltage withstand capability of Quilt Packaging and integrate to vertical WBG devices
  - Simulate RF coupler in Ansys HFSS and integrate to amplitude modulation scheme
  - Optimize and prototype isolated DC/DC converter

Any proposed future work is subject to change based on funding levels